



# Sierra Components, Inc.

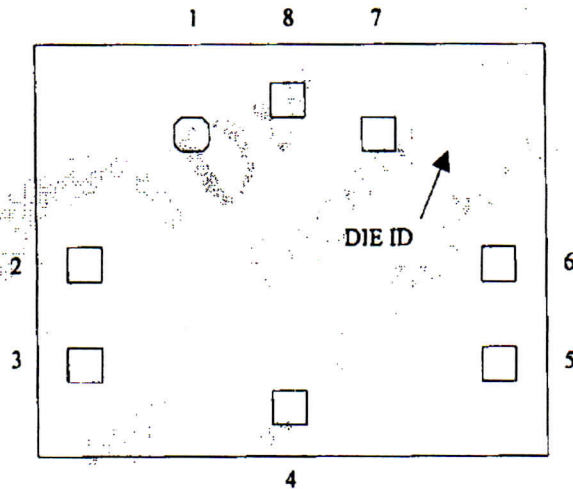
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Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

### PAD FUNCTIONS

- 1 V<sub>OUT1</sub>
- 2 V<sub>INV1</sub>
- 3 V<sub>NON-INV1</sub>
- 4 V<sub>CC-</sub>
- 5 V<sub>NON-INV2</sub>
- 6 V<sub>INV2</sub>
- 7 V<sub>OUT2</sub>
- 8 V<sub>CC+</sub>



**Top Material: Al**  
**Backside Material: Silicon**  
**Bond Pad Size: .004" X .004" min.**  
**Backside Potential: Floating**  
**Mask Ref:**

**APPROVED BY: DK**

**DIE SIZE .037 X .044"**

**DATE: 5/9/16**

**MFG: National Semi.**

**THICKNESS .010"**

**P/N: LMH6715**